

# BoT-nLE522

DATASHEET

CONFIDENTIAL INFORMATION

# List of Contents

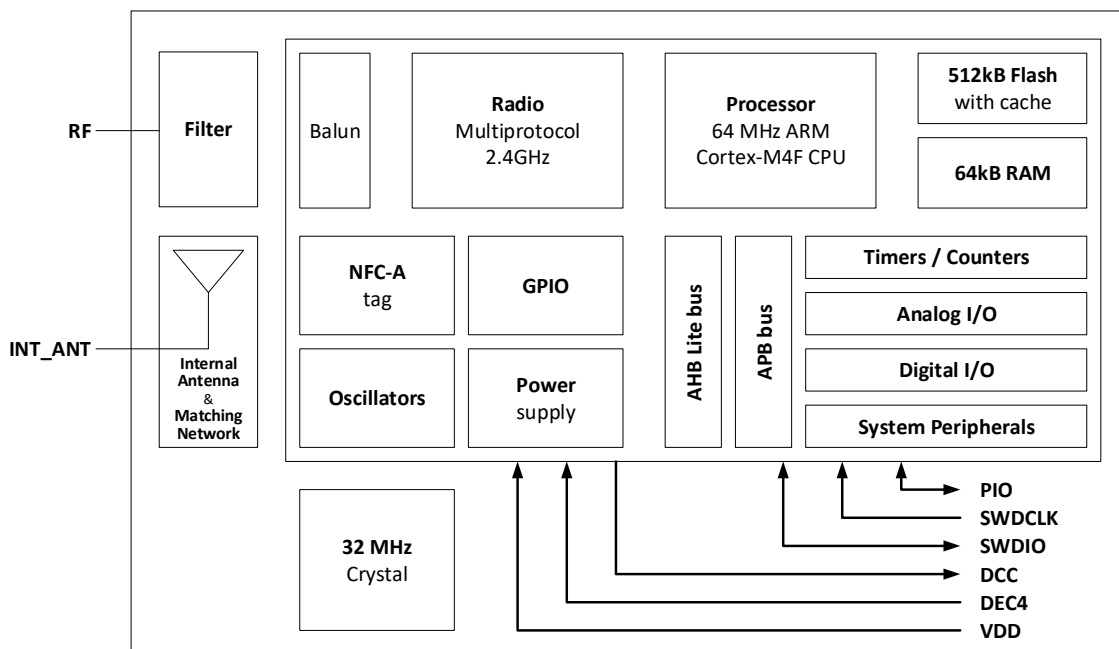
<b>1. General .....</b>	<b>3</b>
1.1 Overview .....	3
1.2 Features .....	4
1.3 Application .....	4
1.4 Pin Configuration .....	5
1.5 Device Terminal Functions .....	6
1.6 Package Dimensions & Land Pattern .....	7
<b>2. Characteristics .....</b>	<b>9</b>
2.1 Electrical Characteristics .....	9
2.2 RF Characteristics .....	11
<b>3. Terminal Description.....</b>	<b>12</b>
3.1 Regulator.....	12
3.2 32.768KHz Crystal Oscillator .....	13
<b>4. Power Consumption.....</b>	<b>15</b>
<b>5. Antenna .....</b>	<b>16</b>
5.1 Antenna Layout Guide .....	16
5.2 Internal Antenna Layout Guide.....	17
5.3 Recommended Module Mounting.....	18
<b>6. Reflow Temperature Profile .....</b>	<b>20</b>
<b>7. Application Schematic.....</b>	<b>21</b>
7.1 Reference Application.....	21
7.2 Internal ANT. / 3.3V UART Application .....	21
7.3 Internal ANT. / 5.0V UART Application .....	21
7.2 External ANT. / 3.3V UART Application.....	21

# 1. General

## 1.1 Overview

The BoT-nLE522 module is a cost-effective, low-power, true system-on-chip (SoC) for Bluetooth Smart (Bluetooth low energy) applications. It enables robust BLE master or slave nodes to be built with very low total bill-of-material costs. BoT-nLE522 combines an excellent RF transceiver with an industry-standard enhanced Cortex-M4F CPU, in-system programmable flash memory, 64kB RAM, and many other powerful supporting features and peripherals. The BoT-nLE522 is suitable for systems where very low power

consumption is required. Very low-power sleep modes are available. Short transition times between operating modes further enable low power consumption.



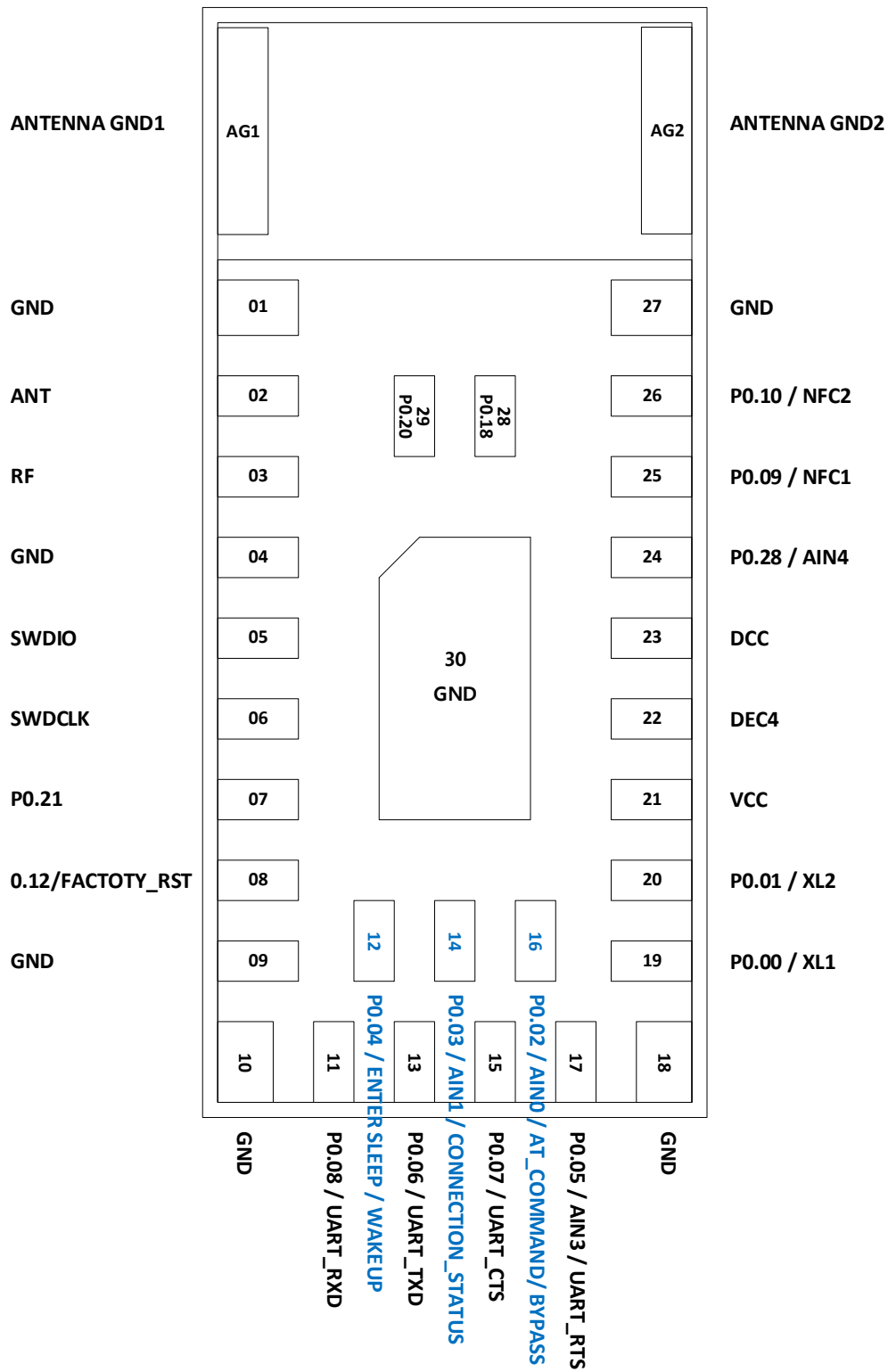
## 1.2 Features

- Bluetooth® v4.2 specification compliant
- Built in Antenna Bluetooth Smart (Bluetooth Low Energy) Module.
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
- Memory: 512 kB Flash/64 kB RAM
- RF Output Power: MAX +4 dBm (-20 ~ 4 dBm)
- RF Receive Sensitivity: -96 dBm
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touch to-pair capabilities
- Fully automatic LDO and DC/DC regulator system (Used LDO by Default)
- Temperature Sensor
- UART (CTS/RTS) with EasyDMA, SPI, and I2C data interfaces.
- 12-Bit 200 ksps ADC with - 8 configurable channels with programmable gain
- Size: 5 mm x 11 mm x 1.63 mm
- Operating Voltage: 1.7V to 3.6V
- Operating Temperature: -40 to +85°C
- RoHS compliant

## 1.3 Application

- 2.4 GHz Bluetooth Low Energy Systems
- Human-Interface Devices
- Sports and Leisure Equipment
- Mobile Phone Accessories
- Consumer Electronics

### 1.4 Pin Configuration



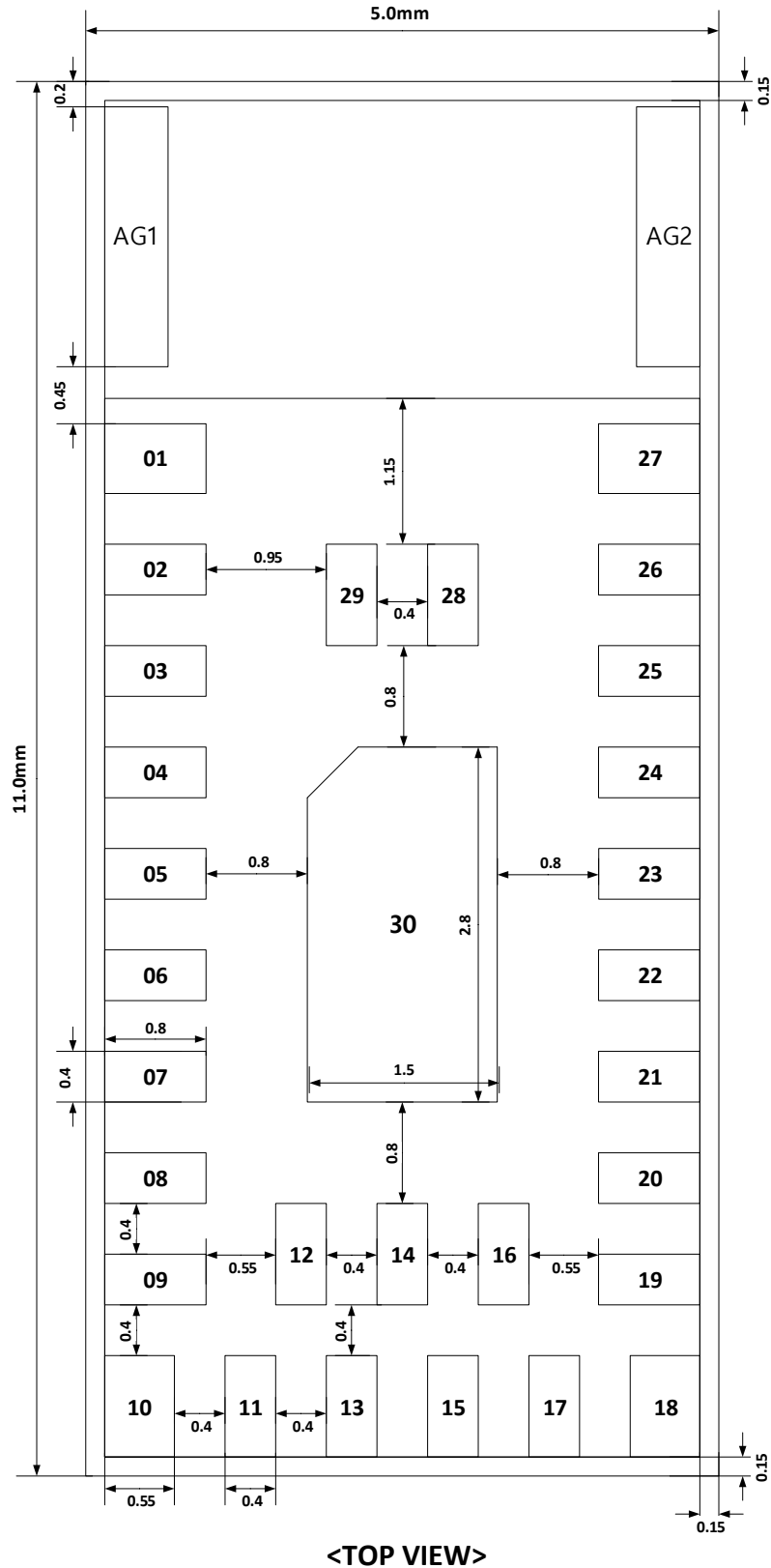
**Pin Configuration (TOP VIEW)**

## 1.5 Device Terminal Functions

Pin No.	Pin Name	Pin Function	Description
01	GND	GROUND	Ground Pin.
02	INT_ANT	INTERNAL ANTENNA IN / OUT	Internal antenna. It should be connected to Pin 02 RF for normal operation.
03	RF	RF IN / OUT PORT	Bluetooth 50Ω transmitter output / receiver input
04	GND	GROUND	Ground Pin.
05	SWDIO	DIGITAL I/O	Serial Wire Debug I/O for debug and programming
06	SWDCLK	DIGITAL INPUT	Serial Wire Debug clock input for debug and programming
07	P0.21	DIGITAL I/O	General purpose I/O pin.
08	P0.12	DIGITAL I/O	General purpose I/O pin.
	FACTORY_RST	DIGITAL INPUT	DISCONNECT & FACTORY_RESET
09	GND	GROUND	Ground Pin.
10	GND	GROUND	Ground Pin.
11	P0.08	DIGITAL I/O	General purpose I/O pin.
	RXD	DIGITAL INPUT	UART RXD
12	P0.04	DIGITAL I/O	General purpose I/O pin.
	AIN2	ANALOG INPUT	SAADC/COMP/LPCOMP input
	ENTER_SLEEP /WAKE_UP	DIGITAL INPUT	ENTER_SLEEP / WAKE_UP
13	P0.06	DIGITAL I/O	General purpose I/O pin.
	TXD	DIGITAL OUTPUT	UART TXD
14	P0.03	DIGITAL I/O	General purpose I/O pin.
	AIN1	ANALOG INPUT	SAADC/COMP/LPCOMP input
	CONNECTION STATUS	DIGITAL OUTPUT	CONNECTION STATUS
15	P0.07	DIGITAL I/O	General purpose I/O pin.
	CTS	DIGITAL OUTPUT	UART CTS
16	P0.02	DIGITAL I/O	General purpose I/O pin.
	AIN0	Analog input	SAADC/COMP/LPCOMP input
	AT COMMAND /BYPASS	DIGITAL INPUT	AT COMMAND/BYPASS
17	P0.05	DIGITAL I/O	General purpose I/O pin.
	AIN3	ANALOG INPUT	SAADC/COMP/LPCOMP input
	RTS	DIGITAL INPUT	UART RTS
18	GND	GROUND	Ground Pin.
19	P0.00	DIGITAL I/O	General purpose I/O pin.
	XL1	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)
20	P0.01	DIGITAL I/O	General purpose I/O pin.
	XL2	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)
21	VCC	POWER	Power supply pin.
22	DEC4	POWER	1.3 V regulator supply decoupling Input from DC/DC converter. Output from 1.3 V LDO
23	DCC	POWER	DC/DC regulator output
24	P0.28	DIGITAL I/O	General purpose I/O pin.
	AIN4	ANALOG INPUT	SAADC/COMP/LPCOMP input
25	P0.09	DIGITAL I/O	General purpose I/O pin.
	NFC1	NFC INPUT	NFC antenna connection
26	P0.10	DIGITAL I/O	General purpose I/O pin.
	NFC2	NFC INPUT	NFC antenna connection
27	GND	GROUND	Ground Pin.
28	P0.18	DIGITAL I/O	General purpose I/O pin.
29	P0.20	DIGITAL I/O	General purpose I/O pin.
30	GND	GROUND	Ground Pin.
AG1	GND	GROUND	Internal antenna Ground 1 Pin.
AG2	GND	GROUND	Internal antenna Ground 2 Pin.

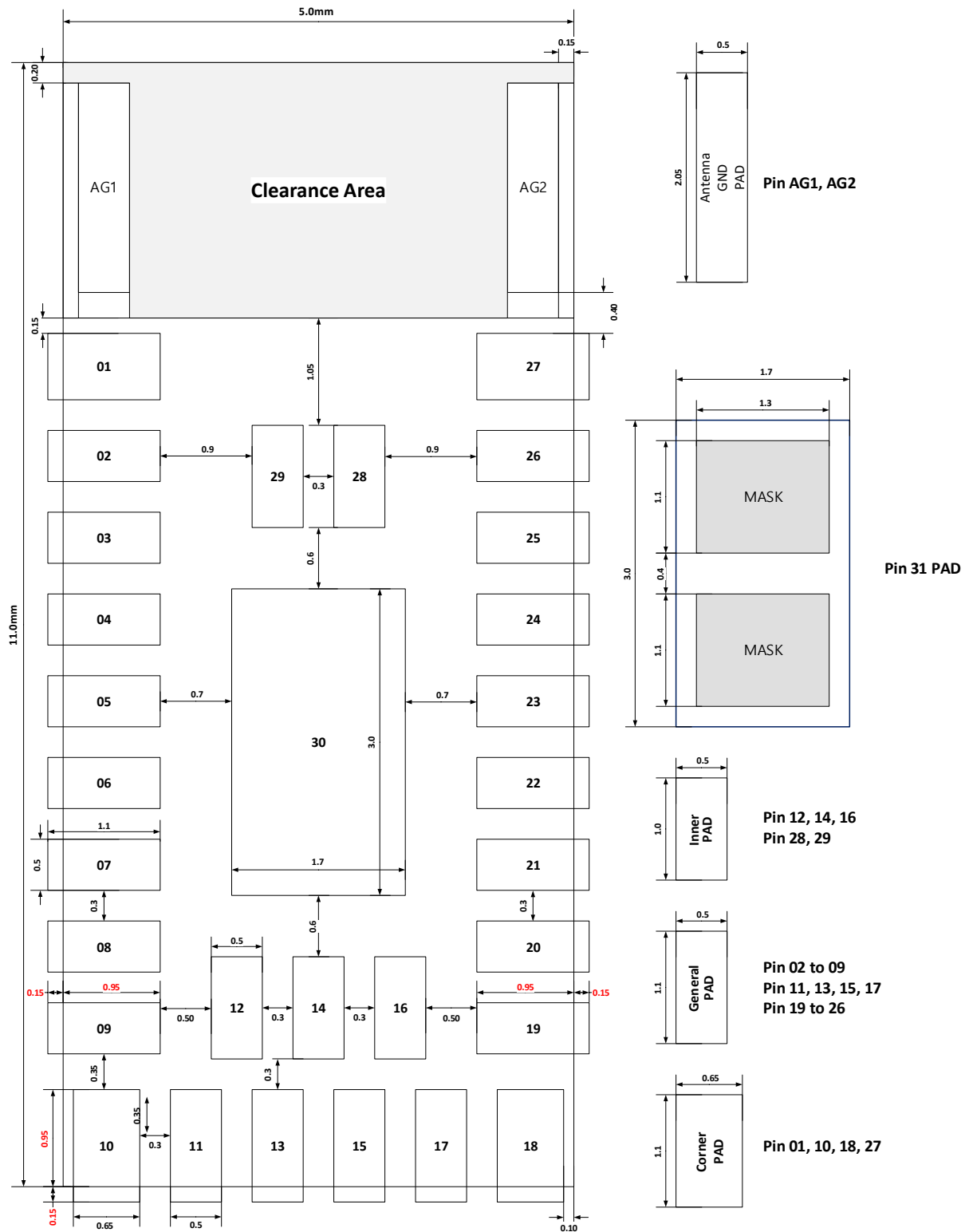
## 1.6 Package Dimensions & Land Pattern

- unit = mm
- General Tolerances =  $\pm 0.2\text{mm}$



<TOP VIEW>

● unit = mm



< Land Pattern (Top View) >



## 2. Characteristics

### 2.1 Electrical Characteristics

#### ■ Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
VDD		-0.3	+3.9	V
GND			0	V
V <sub>I/O</sub> , VDD ≤ 3.6V		-0.3	VDD + 0.3	V
V <sub>I/O</sub> , VDD > 3.6V		-0.3	+3.9	V
Storage temperature		-40	+125	°C
Radio	RF Input Level		10	dBm
MSL	Moisture Sensitivity Level		1	
ESD HBM	Human Body Model		2	kV
ESD CDM	Charged Device Model		500	V
Endurance	Flash Memory Endurance	10000		write/erase cycles
Retention	Flash Memory Retention	10 years		At 40 °C

#### ■ Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	LDO Regulator Operation (Default Mode)	1.7	3.0	3.6	V
VDD	DC/DC Regulator Operation	2.1	3.0	3.6	V
t <sub>r</sub> _VDD	Supply rise time (0V to 1.7V)			60	ms
TA	Operation temperature	-40	25	85	°C

■ DC Characteristics

- The Specification applies for Temperature: 25°C, VDD = 3.0V

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input high voltage	0.7 X VDD		VDD	V
V <sub>IL</sub>	Input low voltage	VSS		0.3 X VDD	V
V <sub>OH,SD</sub>	Output high voltage, standard drive, 0.5 mA, VDD ≥ 1.7	VDD-0.4		VDD	V
V <sub>OH,HDL</sub>	Output high voltage, high drive, 5 mA, VDD ≥ 2.7 V	VDD-0.4		VDD	V
V <sub>OH,HDL</sub>	Output high voltage, high drive, 3 mA, VDD ≥ 1.7 V	VDD-0.4		VDD	V
V <sub>OL,SD</sub>	Output low voltage, standard drive, 0.5 mA, VDD ≥ 1.7	VSS		VSS +0.4	V
V <sub>OL,HDL</sub>	Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V	VSS		VSS +0.4	V
V <sub>OL,HDL</sub>	Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V	VSS		VSS +0.4	V
R <sub>PU</sub>	Pull-up resistance	11	13	16	kΩ
R <sub>PD</sub>	Pull-down resistance	11	13	16	kΩ
I <sub>TX,+4dBm,DCDC</sub>	TX only run current (DCDC, 3V) P <sub>RF</sub> =+4 dBm		7.5		mA
I <sub>TX,+4dBm</sub>	TX only run current P <sub>RF</sub> =+4 dBm		16.6		mA
I <sub>RX,1M,DCDC</sub>	RX only run current (DCDC, 3V) 1Msps		5.4		mA
I <sub>RX,1M</sub>	RX only run current 1Msps		11.7		mA
I <sub>OFF</sub>	System OFF current, no RAM retention		0.3		uA
I <sub>ON</sub>	System ON base current, no RAM retention		1.2		uA
I <sub>RAM</sub>	Additional RAM retention current per 4 KB RAM section		20		nA

## 2.2 RF Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
$f_{OP}$	Operating frequencies	2402		2480	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1Msps		$\pm 250$		kHz
$P_{RF}$	Maximum output power		0	4	dBm
$P_{RFC}$	RF power control range		24		dB
$P_{RFCR}$	RF power accuracy			$\pm 4$	dB
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Msps)		-25		dBc
$P_{RF1,2}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps)		-50		dBc
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
$P_{SENS}$	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER= $1E-3^{17}$		-96		dBm
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		$\pm 2$		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		8		us

## 3. Terminal Description

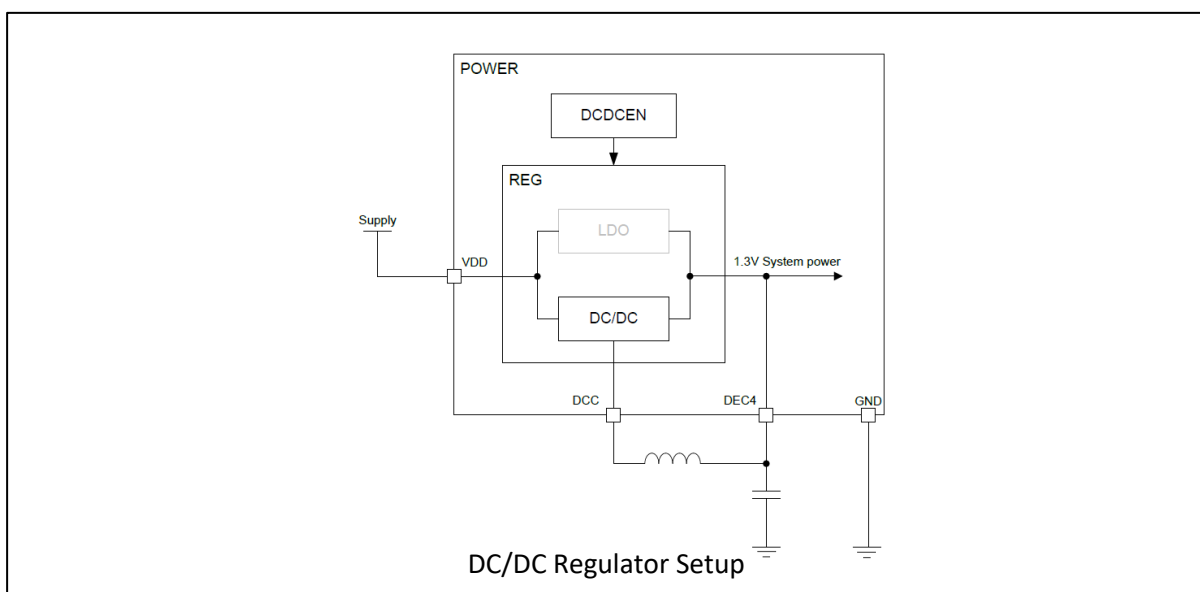
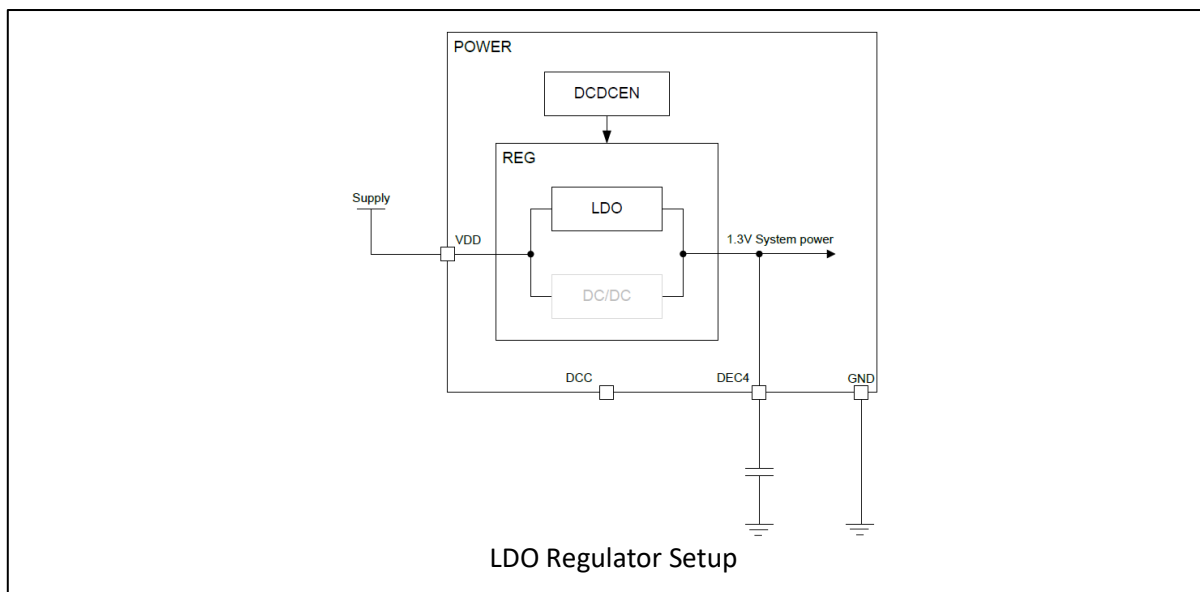
### 3.1 Regulator

The following internal power regulator alternatives are supported:

- Internal LDO regulator
- Internal DC/DC regulator

**The LDO is the default regulator.**

Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in Figure.



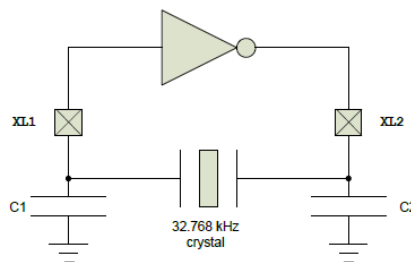
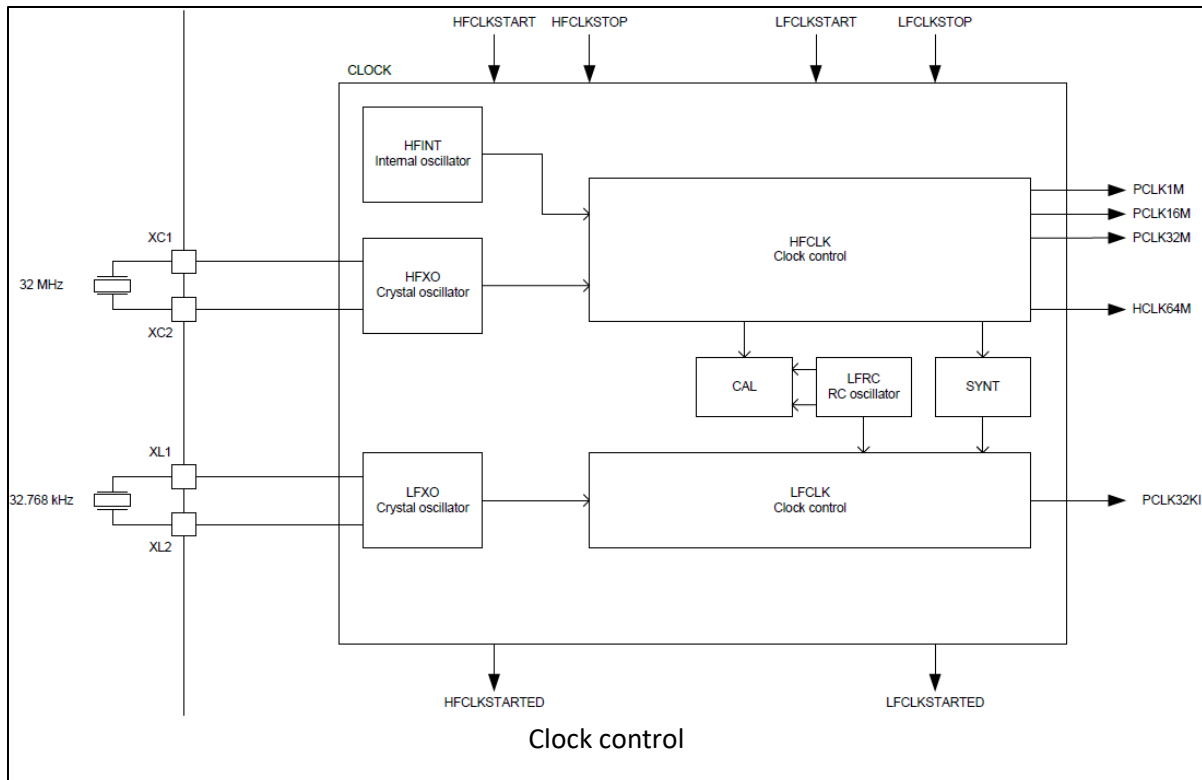
### 3.2 32.768KHz Crystal Oscillator

The BoT-nLE522 external 32.768KHz Crystal does not required for BLE mode

If you choose to use an internal 32.768kHz oscillator, an average of 10uA of current is consumed compared to an external crystal.

The ANT specification requires ± 50ppm accuracy for a 32.768kHz clock. The internal 32.768kHz oscillator may not meet specifications.

BoT-nLE522 F/W does not yet support ANT Mode.



**Circuit diagram of the 32.768 kHz crystal oscillator**

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. Cpcb1 and Cpcb2 are stray capacitances on the PCB.

■ 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_LFRC}}$	Nominal frequency		32.768		kHz
$f_{\text{TOL\_LFRC}}$	Frequency tolerance		$\pm 2$		%
$f_{\text{TOL\_CAL\_LFRC}}$	Frequency tolerance for LFRC after calibration		$\pm 250$		ppm

■ 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{NOM\_LFXO}}$	Crystal frequency		32.768		kHz
$f_{\text{TOL\_LFXO\_BLE}}$	Frequency tolerance requirement for BLE stack		$\pm 250$		ppm
$f_{\text{TOL\_LFXO\_ANT}}$	Frequency tolerance requirement for ANT stack		$\pm 50$		ppm
$C_{\text{L\_LFXO}}$	Load capacitance			12.5	pF
$C_{\text{O\_LFXO}}$	Shunt capacitance			2	pF
$R_{\text{S\_LFXO}}$	Equivalent series resistance			100	
$P_{\text{D\_LFXO}}$	Drive level			1	
$C_{\text{pin}}$	Input capacitance on XL1 and XL2 pads		4		

## 4. Power Consumption

UART State		UART OFF		
BoT State	UART ON(μA)	Internal Pull-Down	External Pull-Down 470K	Internal Pull-Down & External Pull-Down 470K
			**Make internal pull-x register to no-pull state using "AT+INTPULLDOWN=OFF" command	
Advertising	2.20mA	257μA	17μA	265μA
Connected	2.33mA	421μA	186μA	427μA
Sleep	N/A	237μA	7μA	248μA

\*\*measure condition

Firmware version : over V0.5.7

Advertising/Connection interval : Default setting

Remote device : Galaxy S8+

\*\*Current can be change by end-user design and remote device

\*\*Sleep current is measured on UART PIO set low

## 5. Antenna

### 5.1 Antenna Layout Guide



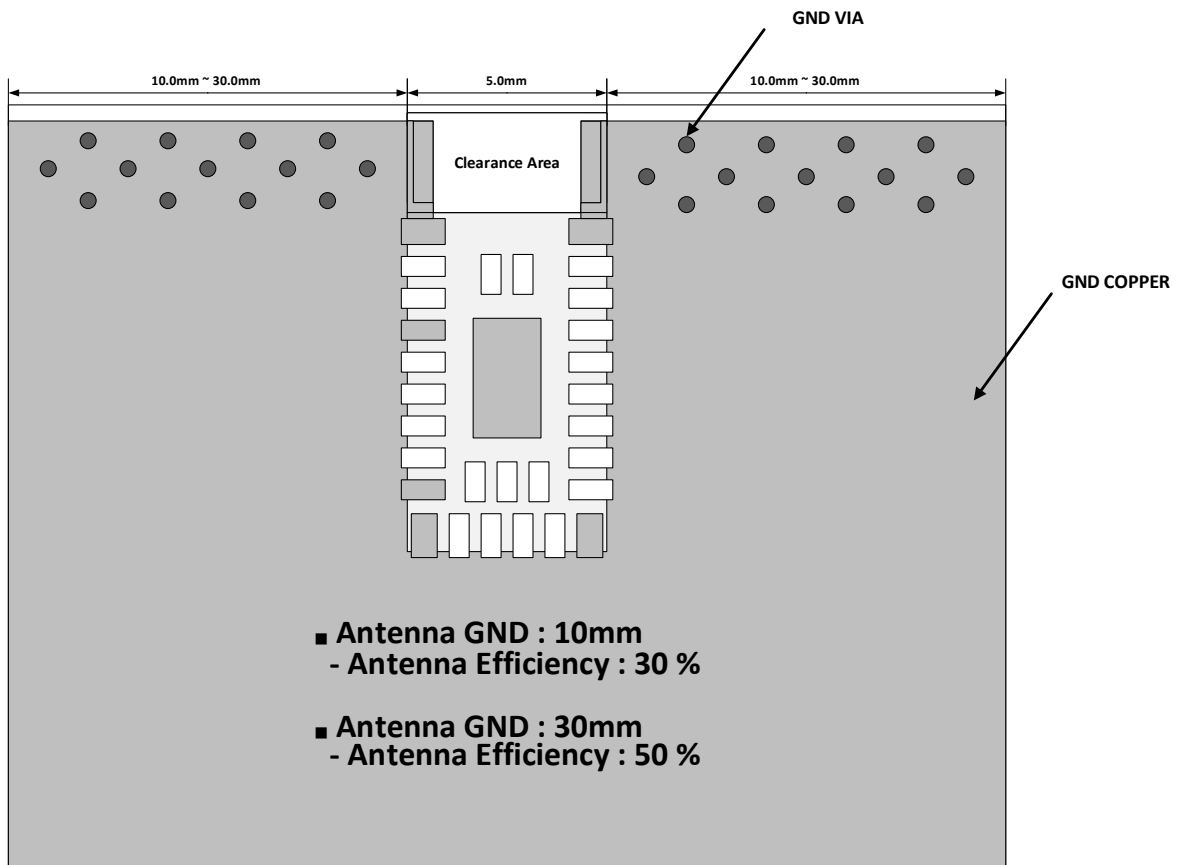


## 5.2 Internal Antenna Layout Guide

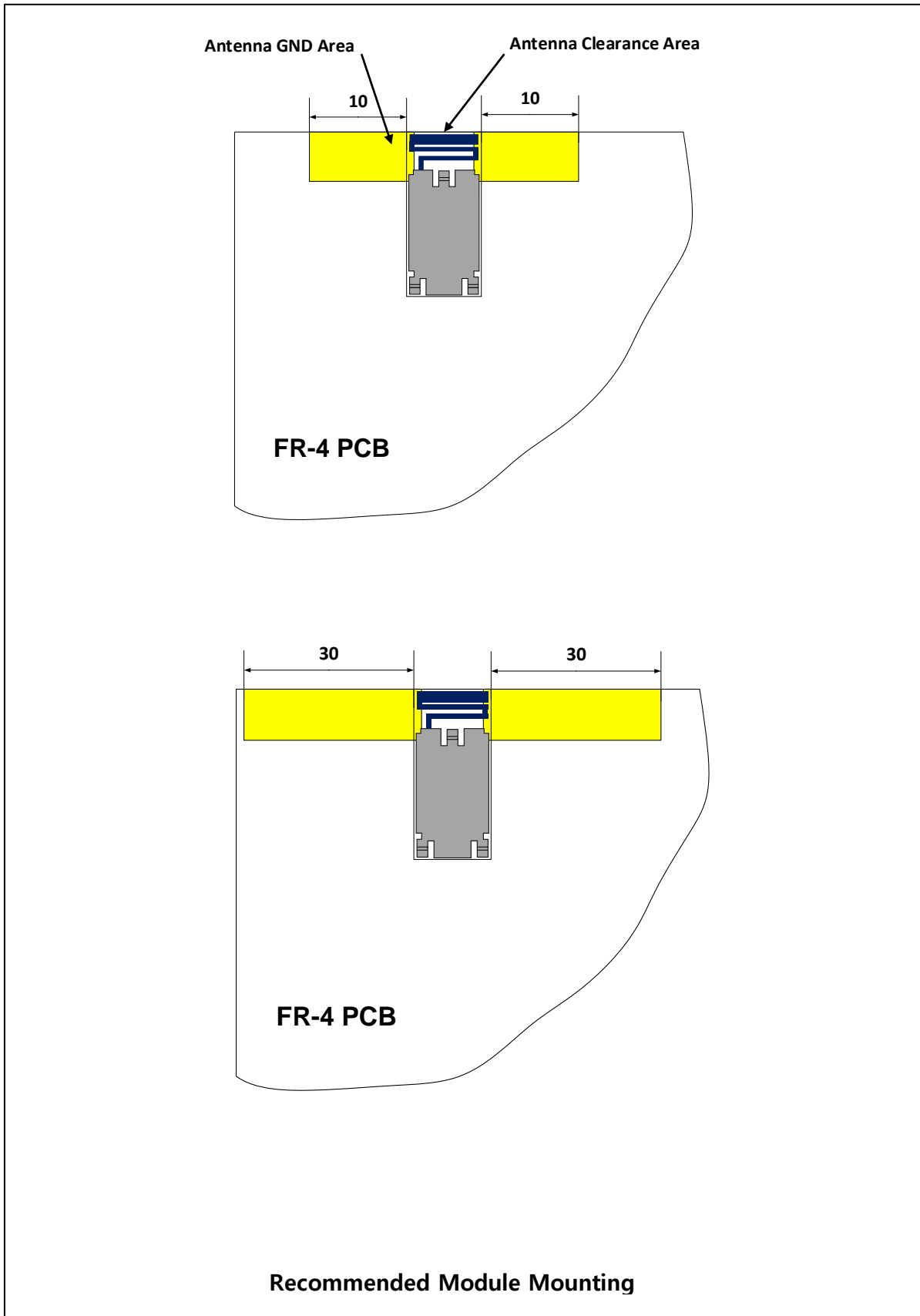
To achieve best radio performance for BoT-nLE522, It is recommended to use the module at the edge of the PCB

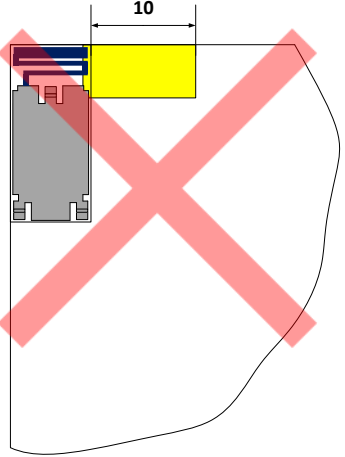
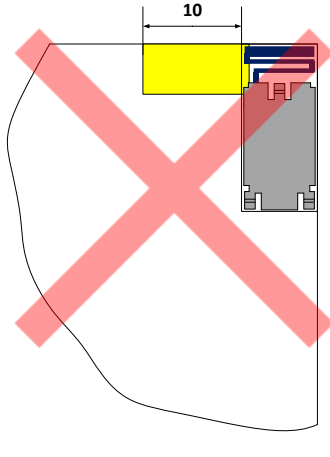
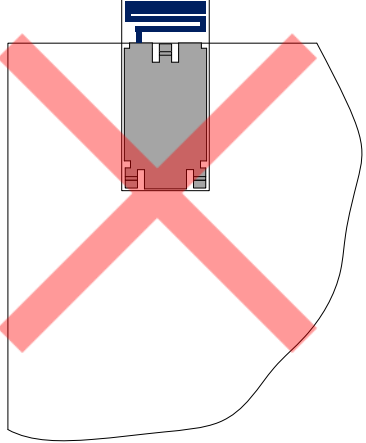
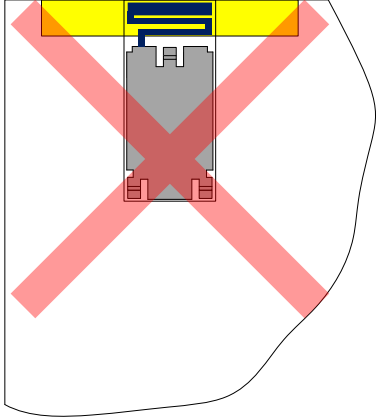
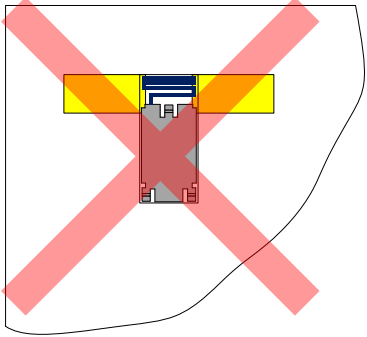
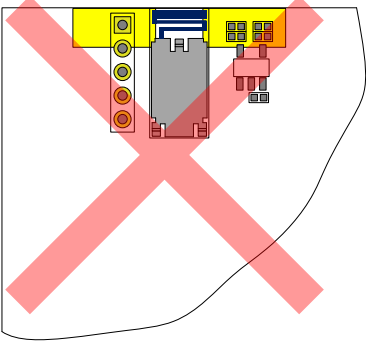
Do not place metal, trace, via, or parts in the Antenna Clearance Area.

AG1, AG2 pins must be connected to GND with flood over. Place the GND vias as close to the GND pins as possible.



### 5.3 Recommended Module Mounting



 <p>한쪽만 Antenna GND 영역이 있는 형태</p>	 <p>한쪽만 Antenna GND 영역이 있는 형태</p>
 <p>Antenna GND 영역이 없고 PCB 외부에 장착된 형태</p>	 <p>Antenna GND 영역을 크기를 임의로 조정 또는 Antenna Clearance 영역에 GND 가 겹치는 형태</p>
 <p>Antenna 영역을 GND 가 둘러싸고 있는 형태</p>	 <p>Antenna GND 영역에 부품이 실장 된 형태</p>
<p><b>Wrong Module Mounting Example</b></p>	

## 6. Reflow Temperature Profile

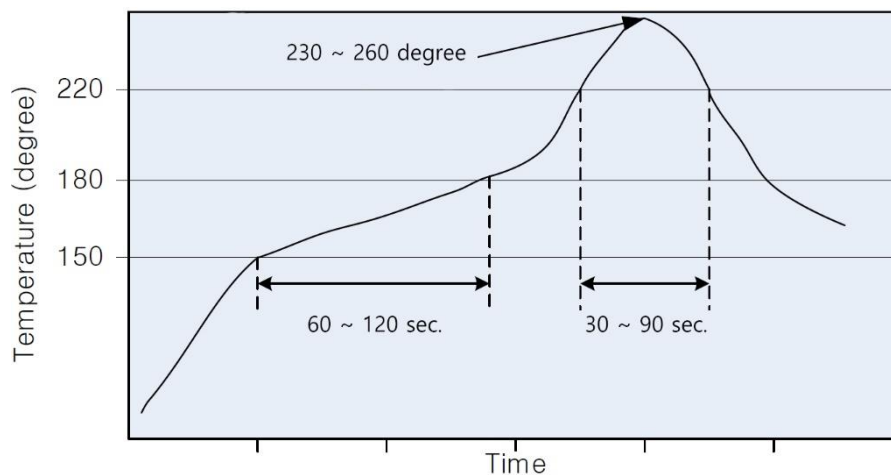
Recommended solder reflow profile are shown in below and follow the lead-free profile I accordance with JEDEC Std 20C.

Table lists the critical reflow temperatures.

Flux residue remaining from board assembly can contribute to electrochemical migration over time.

This depends on number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins.

Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquidus	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max

**WARNING :** For BoT-nLE522

If you have reflow process multiple times in your product, you must be proceed this module in the final reflow process. If not the Shield can will drop out if shield-can adopted .

## 7. Application Schematic

7.1 Reference Application

7.2 Internal ANT. / 3.3V UART Application

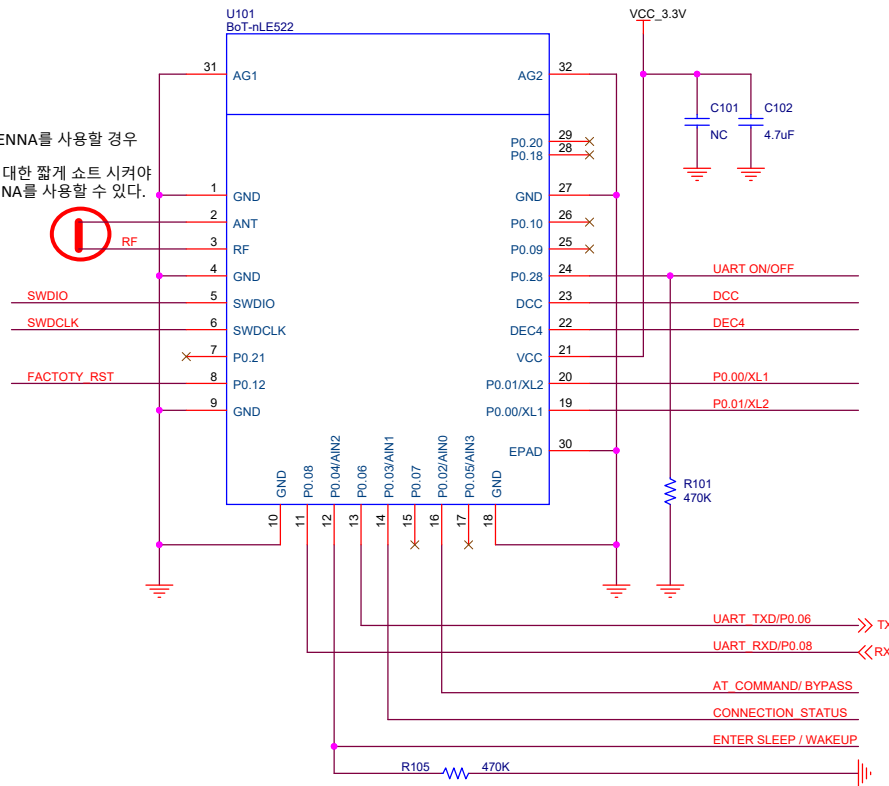
7.3 Internal ANT. / 5.0V UART Application

7.2 External ANT. / 3.3V UART Application

- All reference application are attached next page

# BoT-nLE522 REF. APPLICATION

※ INTERNAL ANTENNA를 사용할 경우  
2PIN 과 3PIN을 최대한 짧게 쇼트 시켜야  
INTERNAL ANTENNA를 사용할 수 있다.



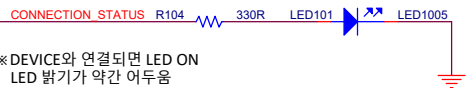
※ External Pull-Down 470K  
Sleep Mode 소모 전류 개선

## CONNECTION\_STATUS LED OPTION

### CONNECTION STATE

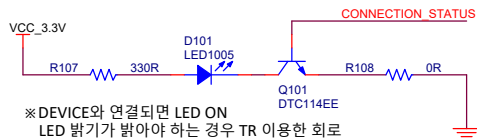
OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

### EXAMPLE 1



※ DEVICE와 연결되면 LED ON  
LED 밝기가 약간 어두움

### EXAMPLE 2



※ DEVICE와 연결되면 LED ON  
LED 밝기가 밝아야 하는 경우 TR 이용한 회로

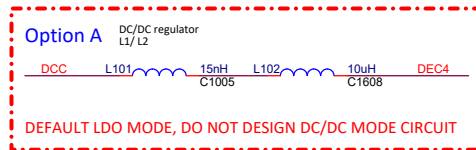
## FACTORY\_RST



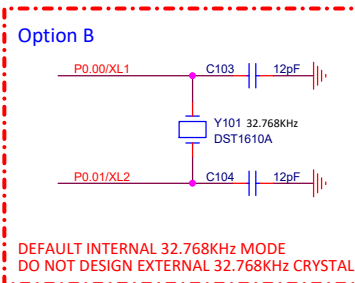
### FACTORY\_RST

DEFAULT SETTING은 INPUT 설정  
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

## OPTION



※ OPTION  
DEFAULT F/W에서 OPTION A / B 지원하지 않음



DEFAULT INTERNAL 32.768KHz MODE  
DO NOT DESIGN EXTERNAL 32.768KHz CRYSTAL

## J-LINK DEBUG PORT



※ Wireless Certification

무선 인증 진행 시 DTM F/W Download Port

## ENTER SLEEP / WAKEUP UART ON/OFF

※ 펌웨어 v0.5.7 이상에서 유효한 기능임

INPUT	ENTER SLEEP / WAKEUP	UART ON / OFF
HIGH(RISING EDGE)	LOW POWER MODE	UART DISABLE
LOW(FALLING EDGE)	WAKE UP & REBOOTING	UART ENABLE

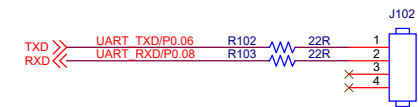
### ENTER SLEEP / WAKE UP

High Level(Rising Edge) 이 감지되면 저전력 모드로 진입이 되며,  
저전력 모드상태에서는 Low Level (Falling Edge) 이 감지되면  
Wake Up 되고 모뎀이 자동으로 재부팅한다.

### UART ON / OFF

High Level(Rising Edge) 이 감지되면 UART가 동작을 멈추고(DISABLE)  
저전력 모드로 진입  
UART DISABLE 상태에서 Low Level (Falling Edge) 이 감지되면 UART 동작이  
재시작(ENABLE)함.

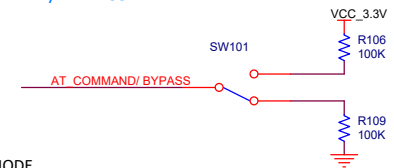
## UART PORT



※ UART Port for SIG / Wireless Certification

무선 인증 진행 시 DTM F/W로 주파수 컨트롤 시 UART를 사용  
반드시 라인 절체할 수 있는 저항 필수 추가

## AT\_COMMAND/ BYPASS



### UART MODE

INPUT	DESCRIPTION
HIGH	AT COMMAND MODE
LOW	BYPASS MODE (DATA MODE)

※ DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※ DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

CHIPSEN Co.,Ltd.  
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해 당 : 1999-6885  
사무실 : 1999-6005



Title  
**BoT-nLE522 REF. APPLICATION**

Size A3 Document Number BoT-nLE522 REF. APPLICATION Rev 1.0

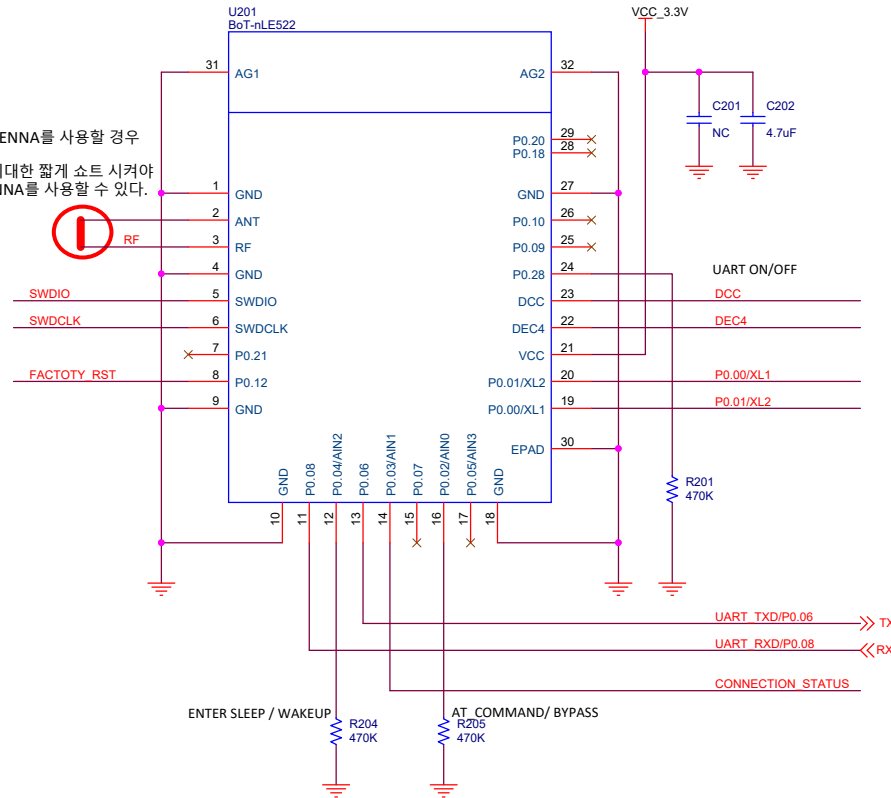
Date: Wednesday, December 11, 2019 Sheet 1 of 4

# BoT-nLE522 REF. APPLICATION - UART 3.3V level input

## Example Schematic

- INTERNAL ANTENNA
- UART 3.3V level input
- Bypass in Bluetooth connected state
- Default LDO Mode
- Default Internal 32.768KHz Mode
- UART ON
- WAKE UP

※ INTERNAL ANTENNA를 사용할 경우  
2PIN 과 3PIN을 최대한 짧게 쇼트 시켜야  
INTERNAL ANTENNA를 사용할 수 있다.

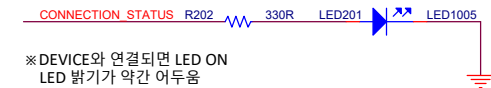


## CONNECTION\_STATUS LED OPTION

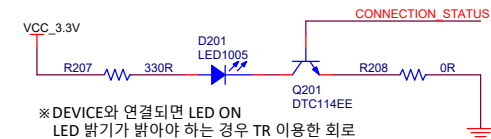
### CONNECTION STATE

OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

### EXAMPLE 1



### EXAMPLE 2



## FACTORY\_RST



DEFAULT SETTING은 INPUT 설정  
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

## J-LINK DEBUG PORT



## ENTER SLEEP / WAKEUP

※ WAKE UP

LOW INPUT : 저전력 모드로 들어가지 않고 동작상태

## UART ON/OFF

※ UART ON

LOW INPUT : UART ON (ENABLE) 상태

## UART PORT



## AT\_COMMAND/ BYPASS

※ BYPASS MODE

LOW INPUT : BYPASS MODE (DATA 전송 모드)

※ DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※ DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

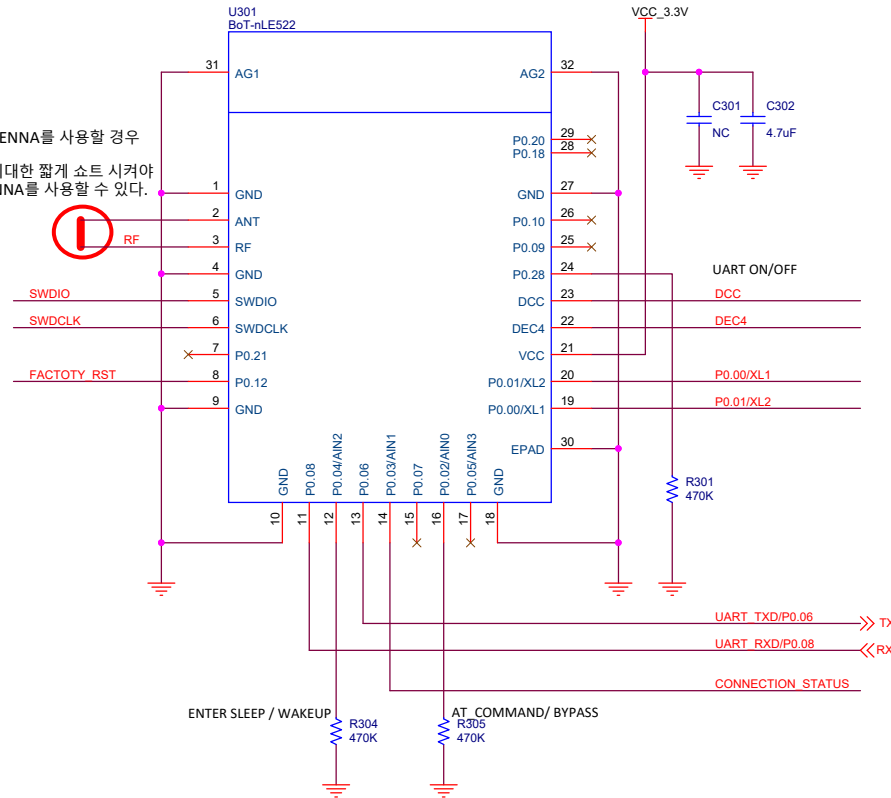
<b>CHIPSEN Co.,Ltd.</b> www.chipsen.com 해 장 : 1599-6885 사무실 : 1599-6005		
Title <b>BoT-nLE522 REF. APPLICATION</b>		
Size A3	Document Number INTERNAL ANT. / UART ON / UART 3.3V	Rev 1.0
Date:	Monday, December 09, 2019	Sheet 2 of 4

# BoT-nLE522 REF. APPLICATION - UART 5V level input

## Example Schematic

- INTERNAL ANTENNA
- UART 5V level input
- Bypass in Bluetooth connected state
- Default LDO Mode
- Default Internal 32.768KHz Mode
- UART ON
- WAKE UP

※ INTERNAL ANTENNA를 사용할 경우  
2PIN 과 3PIN을 최대한 짧게 쇼트 시켜야  
INTERNAL ANTENNA를 사용할 수 있다.

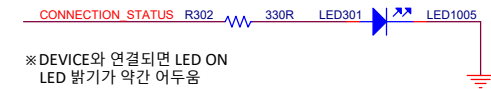


### CONNECTION\_STATUS LED OPTION

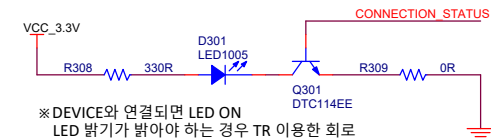
#### CONNECTION STATE

OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

#### EXAMPLE 1



#### EXAMPLE 2



### FACTORY\_RST



DEFAULT SETTING은 INPUT 설정  
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

### J-LINK DEBUG PORT



### ENTER SLEEP / WAKEUP

※ WAKE UP

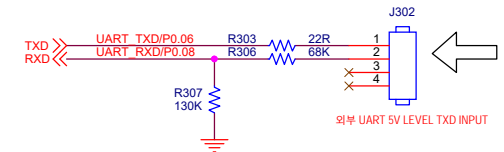
LOW INPUT : 저전력 모드로 들어가지 않고 동작상태

### UART ON/OFF

※ UART ON

LOW INPUT : UART ON (ENABLE) 상태

### UART PORT



### AT\_COMMAND/ BYPASS

※ BYPASS MODE

LOW INPUT : BYPASS MODE (DATA 전송 모드)

※ DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※ DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

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Title: **BoT-nLE522 REF. APPLICATION**

Size: A3	Document Number: INTERNAL ANT. / UART ON / UART 5V	Rev: 1.0
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Date: Monday, December 09, 2019 Sheet 3 of 4



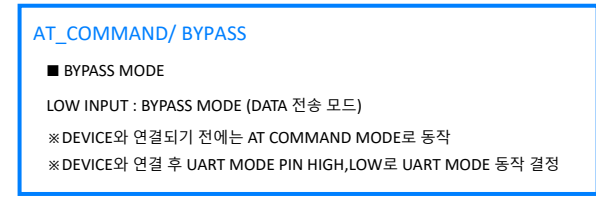
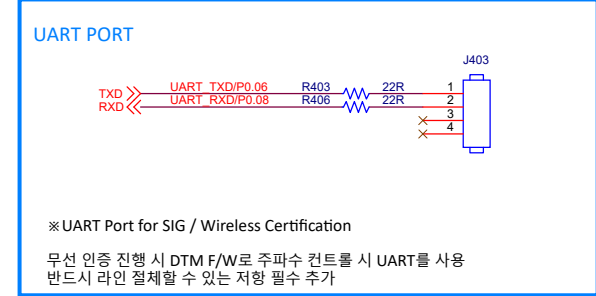
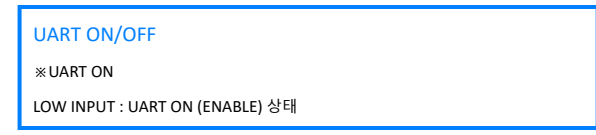
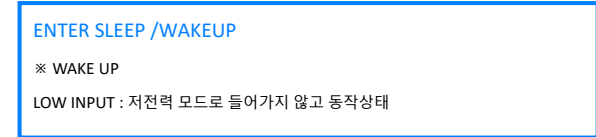
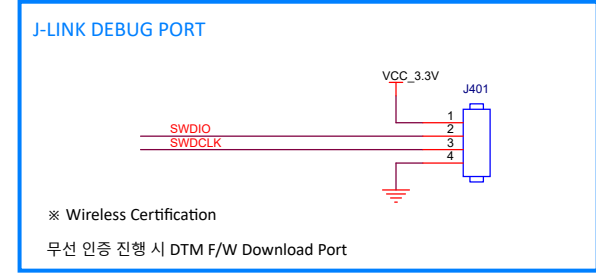
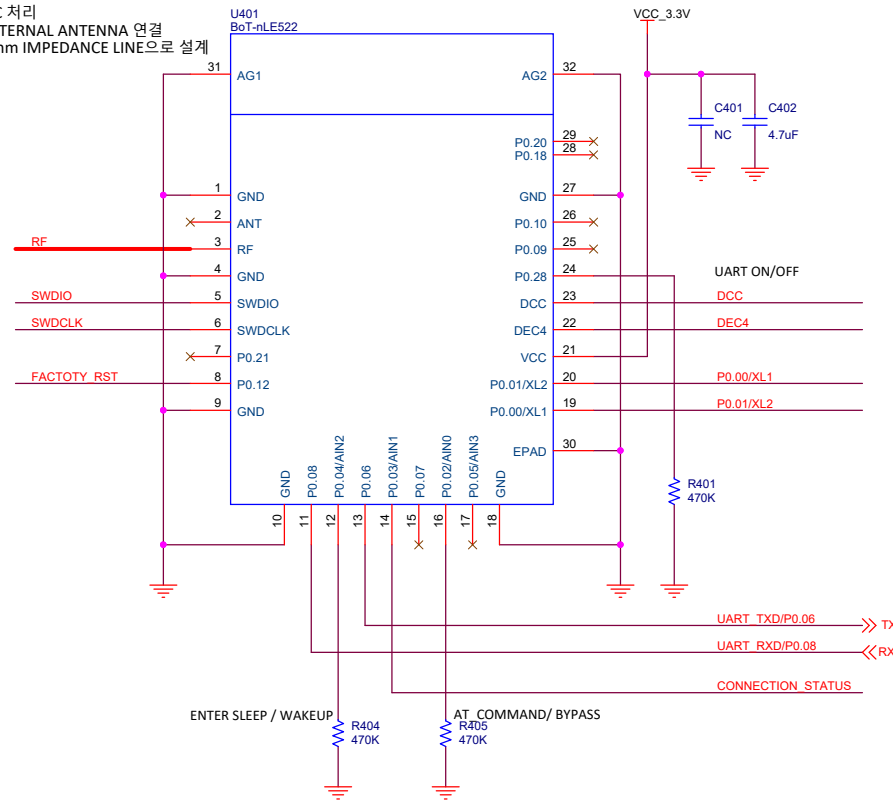
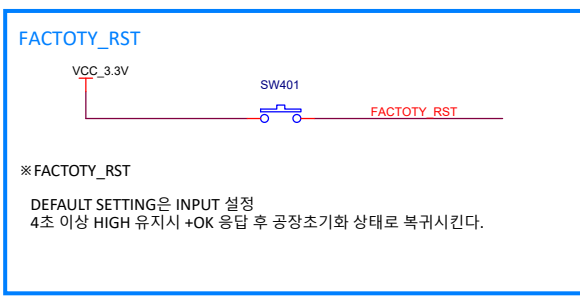
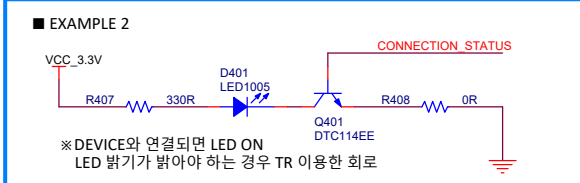
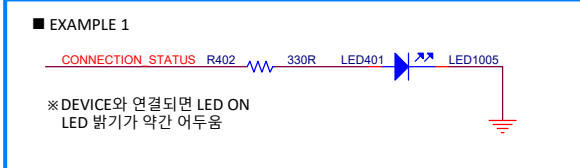
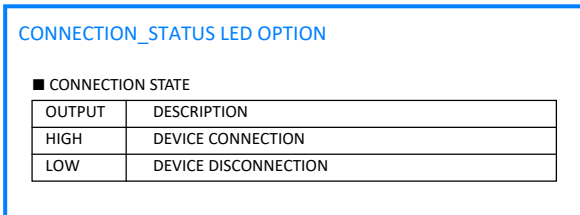
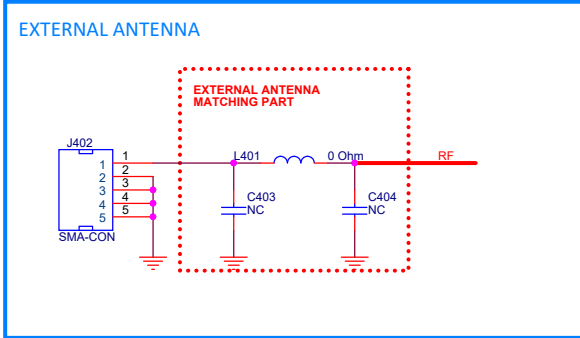
# BoT-nLE522 REF. APPLICATION - EXTERNAL ANTENNA / UART 3.3V LEVEL INPUT

## Example Schematic

- EXTERNAL ANTENNA
- UART 3.3V level input
- Bypass in Bluetooth connected state
- Default LDO Mode
- Default Internal 32.768KHz Mode
- UART ON
- WAKE UP

※ EXTERNAL ANTENNA를 사용할 경우

- 2 PIN(ANT) 은 NC 처리
- 3 PIN(RF)에서 EXTERNAL ANTENNA 연결
- RF LINE은 50 Ohm IMPEDANCE LINE으로 설계



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Size: A3	Document Number: EXTERNAL ANT. / UART ON / UART 3.3V	Rev: 1.0
Date: Monday, December 09, 2019	Sheet: 4	of 4